

## Magma Talus and Quartz Software Qualified for 40-Nanometer Process Technology in TSMC Reference Flow 9.0

*Magma® Design Automation Inc. (Nasdaq: LAVA), a provider of chip design software, today announced that Magma's Talus® IC implementation, Quartz® SSTA statistical analysis, Quartz DFM, Quartz LVS and SiliconSmart® DFM can be accessed through TSMC Reference Flow 9.0. The tools support TSMC's Active Accuracy Assurance initiative, which defines standards of accuracy for all partners in TSMC's design ecosystem. With Magma software and TSMC's Reference Flow 9.0, designers have a proven path from specification to tapeout for 40-nanometer (nm) designs.*

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'Magma is pleased to continue to work with TSMC to enable designers to address the growing complexity, power reduction requirements and time-to-market challenges of analog and digital ICs,' said Kam Kittrell, general manager of Magma's Design Implementation Business Unit. 'With a focus on power, statistical timing analysis and design for manufacturability (DFM), Reference Flow 9.0 and Magma software provide an effective solution for 40 nm and below.'

'Over the past year we have worked with Magma to improve manufacturability of nanometer design accuracy,' said S.T. Juang, senior director of design infrastructure marketing at TSMC. 'Magma Talus and Quartz tool suites have qualified for Reference Flow 9.0 to support the Unified Power Format, DFM and half-node design requirements for TSMC's most advanced process node.'

The Magma software and Reference Flow 9.0 address new design challenges of TSMC's 40-nm process technology. New features include Unified Power Format (UPF) support, transparent half-node design, new statistical on-chip variation (OCV) analysis features and hierarchical DFM capabilities.

### **Addressing Power throughout the Flow with Advanced Techniques and UPF Support**

Working in conjunction with Magma's IC implementation system, Talus Power Pro performs all the innovative power reduction techniques associated with Reference Flow 9.0. Unlike traditional approaches to power management that require multiple tools and use of custom techniques, the Magma system enables continuous, on-the-fly tradeoffs between power and timing throughout the RTL-to-GDSII flow. Having been instrumental in its development, Magma has ensured that Talus Power Pro supports the UPF.

### **Integrated Magma Flow Streamlines Migration to 40-nm Process**

Reference Flow 9.0 delivers transparent half-node design support for the latest 40-nm process technology. Since the Magma software is tightly integrated and based on a unified data model, it can minimize the introduction of new errors and enables a clean handoff for the half-node design.

### **Robust Statistical Timing Analysis**

Magma and TSMC have developed one of the most robust statistical static timing analysis (SSTA) methodologies to reduce excess design margins, optimize design performance and increase yields.

Based on Magma's Quartz SSTA, this methodology supports global (inter-die) and random (intra-cell) process variations, composite current source (CCS) models, statistical leakage analysis and statistical optimization, as well as design-specific on-chip variance derived from statistical analysis.

### **Integrated Characterization-to-Silicon DFM Flow**

The complexity of 40-nm and below manufacturing requires additional foundry process data to improve model accuracy. Magma provides a comprehensive characterization-to-silicon DFM flow based on SiliconSmart DFM for model characterization, Talus Vortex for design implementation and Quartz DFM for advanced model-based DFM. Magma provides an integrated flow that combines model- and rule-based approaches to better address variability and minimize systematic and parametric yield loss. With this flow, users can accurately predict, prevent and correct DFM-related problems to tape out faster, achieve higher yields and reduce design pessimism. Handoff to manufacturing is also simplified because sign-off-accurate DFM compliance checks are performed within the implementation flow.

New for Reference Flow 9.0, Magma offers a comprehensive physical and electrical DFM solution that leverages TSMC's advanced DFM modeling to address potential parametric performance shifts due to process variation. Quartz LVS supports a new table-based DFM-LPE extraction flow that accurately generates transistor parameters to account for manufacturing effects, including silicon printability. Magma's chemical mechanical polishing (CMP)-aware thickness-based extraction uses the new TSMC VCMP engine and the Thickness-to-Electrical (T2E) flow to provide feature-scale (within grid) accuracy, as well as a new T2E Detector that complements the existing VCMP compliance checks. Quartz DFM works with a TSMC-certified lithography simulator that drives the enhanced TSMC Shape-to-Electrical (S2E) engine providing silicon accurate Leff and Weff transistor models. Magma has combined this LPC-to-timing flow with Quartz LVS to provide a unique Electrical-DRC (eDRC) capability, providing easy-to-use feedback for IP developers. The integration within Talus Vortex shortens design cycles by anticipating DFM issues early in the flow, resulting in improved design robustness and increased yield.

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### **About Magma**

Magma's software for designing integrated circuits (ICs) is used to create complex, high-performance chips required in cellular telephones, electronic games, WiFi, MP3 players, DVD/digital video, networking, automotive electronics and other electronic applications. Magma's EDA software for IC implementation, analysis, physical verification, circuit simulation and characterization is recognized as embodying the best in semiconductor technology, enabling the world's top chip companies to "Design Ahead of the Curve"™ while reducing design time and costs. Magma is headquartered in San Jose, Calif., with offices around the world. Magma's stock trades on Nasdaq under the ticker symbol LAVA. Visit Magma Design Automation on the Web at [www.magma-da.com](http://www.magma-da.com).

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