

Synplicity Launches ReadyIP program: The industry's first Universal, Secure IP flow for FPGA Implementation

Key IP Vendors—ARM, CAST, Gaisler Research, Synopsys and Tensilica—Support Program

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Synplicity®, Inc. (NASDAQ: SYNP), a leading supplier of innovative IC design and verification solutions, today announced the ReadyIP Initiative, a program that takes aim at simplifying the access, evaluation, and use of intellectual property (IP) for FPGA-based system design. The ReadyIP program delivers the industry's first and complete universal, encrypted design methodology for FPGA implementation, allowing users to incorporate and easily integrate IP from several third-party vendors within their designs using the Synplify Pro® and/or Synplify® Premier solutions, Synplicity's industry-standard synthesis environments.

The ReadyIP initiative comprises a number of key elements. These include standards-based IP encryption with rights management to facilitate easy evaluation of IP; the System Designer™, a new technology-independent IP integration capability that is now part of Synplicity's synthesis products (see related announcement, *Synplicity Introduces System Designer: System-level Implementation and IP Integration Tool For FPGA Design*); 'push-button' Internet access to third-party IP directly from within Synplicity's FPGA design environment; and the use of the SPIRIT Consortium's IP-XACT IP packaging format to enable mix and match of IP from a variety of sources including the use of in-house IP.

Synplicity also announced that its ReadyIP initiative is being endorsed and supported by leading IP vendors. ARM, CAST, Gaisler Research and Tensilica are partnering with Synplicity as charter members in this new industry initiative. Selected secure IP from these vendors, that universally target multiple FPGA devices, will be available through this new program.

Synplicity believes its ReadyIP program is a big step toward providing an industry-wide, standards-based design flow for FPGA implementation using IP which benefit users because they can: 1) try IP before having to license it, 2) improve design productivity when using IP, and 3) use the standards to create their own IP-based design reuse practice.

'Synplicity's ReadyIP Program is the first to facilitate the widespread availability of IP while allowing designers to easily 'try before they buy' third-party IP,' said Andy Haines, senior vice president of marketing, Synplicity. 'As important, it allows a company to package its own IP and securely distribute it throughout an organization for design reuse and implementation using Synplicity's ReadyIP design flow.' Haines continued, 'We are very pleased to welcome ARM, CAST, Gaisler Research, Synopsys and Tensilica into this program not only because they are key IP suppliers, but also as forward thinking companies supporting this major productivity advancement for the design community.'

FPGA designers are increasingly turning to third-party IP to implement FPGA-based systems. The ReadyIP solution now gives these designers access to both third-party and internally developed IP within Synplicity's FPGA synthesis products and simplifies IP assembly through Synplicity's System Designer capability, a solution for integrating IP into FPGA designs using the designer's FPGA of

choice. IP access is provided through Synplicity's synthesis environment via a Web browser. With this 'push-button' feature, the user can download various IP directly into the synthesis environment for evaluation.

According to Mary Olsson, chief analyst with Gary Smith EDA, 'ReadyIP is a smart solution that gives users the flexibility to implement designs using various FPGA devices best suited to their particular applications. Moreover, users easily will be able to migrate their designs as new generations of technology emerge. By founding this vendor independent design flow on industry standards, and with great lead IP partners, Synplicity has really strengthened the value proposition of this new initiative.'

'Synplicity's ReadyIP program is unique in that it offers FPGA designers easy and efficient access to the IP options available today, including the ARM® Cortex™-M1 processor,' said Graham Budd, EVP and general manager, Processor Division, ARM. 'We believe ReadyIP will offer designers a better user experience and the ability to complete their designs more quickly and efficiently and deploy them on any FPGA they choose.'

'The standards-based ReadyIP program brings a whole new level of IP accessibility right to the FPGA designers who need it the most,' said Hal Barbour, president of CAST. 'We've been a pioneer in the effective use of IP cores starting 15 years ago, and are excited to help expand the realm of technology independence for FPGA designers through this partnership with Synplicity.'

'Synplicity's ReadyIP initiative will help rapidly expand usage of IP by FPGA designers, thereby helping grow the IP market as a whole,' said Steve Roddy, Tensilica's vice president of marketing and business development. 'As FPGA designs get larger and more complex, FPGA designers will increasingly turn to IP to increase their design productivity.'

'By providing a universal and safe method to protect third party IP, Synplicity is playing a key role in helping the industry speed the development and verification of complex SoCs,' said John Koeter, senior director of marketing for IP and Services at Synopsys. 'With the ReadyIP program, ASIC and SoC designers can now have a convenient way to prototype their designs in FPGAs.'

The ReadyIP flow encompasses support for the SPIRIT Consortium's IP-XACT industry standard specification for integration and configuration of IP, as well as support for Synplicity's OpenIP encryption methodology that allows IP providers to securely deploy their IP to potential and existing customers. Synplicity has donated this encryption methodology to the IEEE and standardization is now officially in process through the IEEE P1735 Working Group.

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Synplicity®, Inc. (NASDAQ: [SYNP](#)) is a leading supplier of innovative IC design and verification solutions that serve a wide range of communications, military/aerospace, semiconductor, consumer, computer, and other electronic applications markets. Synplicity's FPGA implementation tools provide outstanding performance, cost and time-to-market benefits by simplifying, improving and automating logic synthesis, physical synthesis, analysis and debug for programmable logic designs. Synplicity's ESL synthesis solutions significantly improve productivity for DSP designs realized in ASIC and FPGA devices. The Confirma™; at-speed verification platform, comprising software tools and

the HAPS™ family of prototyping systems, enables both comprehensive verification of ASIC, ASSP and SoC designs and software development prior to chip tapeout. Synplicity is the number one supplier of FPGA synthesis tools and its physical synthesis and ASIC verification technologies are the recipients of several prestigious industry awards. The company operates in more than 20 facilities worldwide and is headquartered in Sunnyvale, California. For more information visit <http://www.synplicity.com>

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